

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

- 1 1. (Previously Presented) An apparatus, comprising:
 - 2 a variable speed bus, the variable speed bus initialized with a first clock
 - 3 frequency;
 - 4 a first unit coupled to the variable speed bus, the first unit having a first rate of
 - 5 requests to access the variable speed bus;
 - 6 a second unit coupled to the variable speed bus, the second unit having a
 - 7 second rate of requests to access the variable speed bus; and
 - 8 an arbitration and bus clock control unit to monitor the first access request rate
 - 9 from the first unit and the second access request from the second unit, and to determine
 - 10 a second clock frequency for the variable speed bus based on at least one of the first
 - 11 access rate and the second access request rate.
- 1 2. (Original) The apparatus of claim 1, wherein the first unit is a processor unit.
- 1 3. (Original) The apparatus of claim 1, wherein the second unit is a video processor
- 2 unit.
- 1 4. (Original) The apparatus of claim 1, wherein the first unit is a hard disk drive
- 2 controller unit.

1 5. (Original) The apparatus of claim 1, wherein the second unit is an isochronous data
2 transfer unit.

1 6. (Canceled).

1 7. (Previously Presented) The apparatus of claim 5, wherein the isochronous data
2 transfer unit is a 1394 controller unit.

1 8. (Previously Presented) The apparatus of claim 5, wherein the isochronous data
2 transfer unit is a USB controller unit.

1 9. (Canceled).

1 10. (Previously Presented) A system, comprising:
2 a device coupled to a variable speed bus, the device having a rate of request to
3 access the variable speed bus; and
4 a clock throttling logic to adjust a clock frequency associated with the variable
5 speed bus based on the rate of request to access the variable speed bus from the
6 device.

1 11. (Previously Presented) The system of claim 10, further comprising:
2 an arbitration and bus control unit to monitor the rate of request to access the
3 variable speed bus from the device and to instruct the clock throttling logic to adjust the
4 clock frequency associated with the variable speed bus the device's rate of request to
5 access the variable speed bus.

1 12. (Original) The system of claim 10, wherein the device coupled to the variable
2 speed bus is a processor.

1 13. (Original) The system of claim 10, wherein the device coupled to the variable
2 speed bus is a video processor.

1 14. (Original) The system of claim 10, wherein the device coupled to the variable
2 speed bus is a hard disk drive controller.

1 15. (Original) The system of claim 10, wherein the device coupled to the variable
2 speed bus is an isochronous data transfer controller.

1 16. (Canceled).

1 17. (Previously Presented) The system of claim 15, wherein the isochronous data
2 transfer controller is a 1394 controller.

1 18. (Previously Presented) The system of claim 15, wherein the isochronous data
2 transfer controller is a USB controller.

1 19-20. (Canceled).

1 21. (Previously Presented) The apparatus of claim 1, further comprising:
2 a clock throttling unit to adjust the clock frequency of the variable speed bus to
3 the second clock frequency according to an instruction from the arbitration and bus
4 clock control unit.

1 22. (Previously Presented) The apparatus of claim 21, wherein the arbitration and bus
2 clock control unit determines the second clock frequency based on a first bandwidth
3 requirement from the first unit and a second bandwidth requirement from the second
4 unit, the first bandwidth requirement derived from the first rate of request to access the
5 variable speed bus from the first unit, the second bandwidth requirement derived from
6 the second rate of request to access the variable speed bus from the second unit.

1 23. (Previously Presented) The apparatus of claim 21, wherein the variable speed bus,
2 the first unit, the second unit, the clock throttling logic and the arbitration and clock
3 control unit are located on a single semiconductor die.

1 24. (Previously Presented) The system of claim 11, wherein the arbitration and bus
2 clock control unit determines a new clock frequency based on a bandwidth requirement
3 from the device, the device's bandwidth requirement derived from the device's rate of
4 request to access the variable speed bus and instructs the clock throttling logic to adjust
5 the clock frequency of the variable speed bus to the new clock frequency.